UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/652,134	08/29/2003	Philip E. May	CML00770D	1156

33117 7590 02/06/2006

LARSON + ASSOCIATES PC
221 EAST CHURCH ST.
FREDERICK, MD 21701

EXAMINER
PAN, DANIEL H

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/652,134	MAY ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/29/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-13 are presented for examination.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the storage or memory which the identifiers and the modified sequence are being stored.

3. Claims 1,6 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: the step for storing the multiple-instruction control words in order to modify the sequence of the multiple-instruction control words to remove the set of aligned fields . It is unclear whether the sequence of the multiple-instruction control words is compressed in a computer readable medium in the processor or , it is directed to a representation of a dataflow of a mere program . If it is directed to compression represented by data flow graph, additional "101" rejection will apply (see following).

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1,6, are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reasons are given below .

5. As to claim 1, and 6, the claims are not directed to a useful, concrete and tangible result because although claim 1 recites a processor in the preamble, no specific element of the processor has been reflected into the body of the claim to support the [processor in preamble. The evidence shows that (see applicant's specification page 6, lines 13-14) a data flow is a representation of entire inner loop computation. This data flow representation could be a mere program. Without a recitation of specific elements of the processor in the body of the claims . It is read as program per se. As to claim 6, clam 6 recites to provide decompressed control word to the processor for execution. However, no execution has been achieved in the claim. Therefore, it is also viewed as a mere program, hence achieves no useful, concrete and tangible result.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 , 4, 5, 6,8,9,10,11,12 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka (5,893,143).

7. As to claim1, 4, 5, Tanaka disclosed a VLIW system including at least :

a) a sequence of multiple-instruction control words (see fig.6) , each control word comprising a plurality of ordered fields [FIELDS] and each ordered field containing an instruction for an element of a processor,

b) identifying a set of aligned fields that contain NOP instructions (see NOPs in the instruction string) in each control words of the sequence of multiple-instruction control words;

c) modifying the sequence of multiple-instruction control words to remove the set of aligned fields (see the fields being removed by mask in fig.6);

d) storing an identifier (see the mask) that identities the set of aligned fields removed; and storing the modified sequence of multiple-instruction control words.

8. As to claim 6, Tanaka also taught :

a) fetching an identifier (see the mask) that identifies a set of aligned fields (see fields in fig.6) removed during compression of the sequence of multiple-instruction control words (see the masked-off fields in fig,6) ;

for each control word of the compressed sequence of multiple-instruction control words;

b) fetching a control word (see read out of instruction);

c) reconstructing a corresponding uncompressed control word by inserting NOP instructions into the compressed control word in accordance with the identifier (see reinserting of NOP into instruction in col.6, lines 1-2, see also the decompression when the instruction was readout in col.3, lines 6-13);

d) providing the decompressed control word to the processor for execution (see the decompressed instruction for executing in col.7, lines 34-38).

9. As to claim 8, see the mask as the identifier in fig.11 for selecting the clusters.

10. As to claim 9, Tanaka also taught identifier [mask] was a compression mask having one bit associated with each field of the multiple-instruction control word (see the bits in mask in fig.6) .

11. As to claim 10, Tanaka taught :

A) a mask latch for storing a compression mask (see mask) that identifies a set of aligned fields removed during compression of the sequence of multiple-instruction control words (see fig.6) ;

b) a logic unit coupled to the mask latch and responsive to the compression mask (see the logic circuit coupled to mask in fig.9 and fig.11);

c) a memory for storing one or more compressed multiple-instruction control words (see fig.6, and fig.9 and fig.11 memory for storing the mask) ;

d) a pipelined permute unit, coupled to the logic unit and the memory and

operable to reconstruct multiple-instruction control words by fetching a compressed multiple-instruction control word from the memory and inserting NOP instructions in accordance with the compression mask (see reinserting of NOP into instruction in col.6, lines 1-2, see also the decompression when the instruction was readout in col.3, lines 6-13) ; and

e) an instruction register coupled the pipelined permute unit and operable to present reconstructed multiple-instruction control words to the processor (see each entry in fig.6).

12. As to claim 11, Tanaka showed a write enabling signal for each memory caches (memory banks). Therefore, Tanaka was able to disable the memory banks.

13. As to claim 12 , see the mask as the identifier in fig.11 for selecting the clusters.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (5,893,143) in view of Mehrotra et al. (6,571,016).

15. As to claim 2, Tanaka did show a loop for computation as claimed. However, Mehrotra disclosed a system including a loop (routine) for computation in a personal computer (e.g. see the decompressing routine used by personal computer in col.7,

lines 46-55). It would have been obvious to one of ordinary skill in the art to use ns in Tanaka for including the loop for computation as claimed because the use of Mehrotra could provide Tanaka the ability to repeat the performance of a specific computation (e.g. the decompression) at subsequent processing cycle, and Tanaka did suggest the need for computation in his decompression system in a personal computer (see adding of 1 to x variable in fig.1, personal computer in col.1), and also suggested the applicability of a loop (see the branch instruction in col.4, lines 22-33). And, It was well recognizable by one of ordinary skill in the art that a branch would return back at the branch point, and therefore, formed a loop, and the calculation x variable of Tanaka could be done in a loop because of the great number of elements X (see fig.1) to be incremented , therefore, provided a motivation.

16. Claim 3, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (5,893,143) in view of Pechanek et al. (6,173,389) .

17. As to claims 3, 13, limitations of parent claims discussed above will not be repeated herein. Tanaka did not specifically show his system was used for vector processing as clamed. However, Pechanek disclosed a system for including a nop operation with a vector processing (e.g. see the background in col.1, lines 35-42). It would have been obvious to one of ordinary skill in the art o use Pechanek in Tanaka for including the vector processing as claimed because the use of Pechanek cold provide Tanaka the capability to adapt to different type of processing methods , such as

vector processing, and it could be done by configuring the vector of Pechanek with a modified parameters (e.g. the vector registers) into Tanaka, so that the vector processing of Pechanek could be recognized by Tanaka, and since no specific type of vector processing is being recited in the claim, one of ordinary skill in the art should be able to recognize the use of vector processing in general into Tanaka for achieving the fast processing capacity as desired by Tanaka (see Tanaka col.3, lines 37-41).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (5,893,143) in view of Shebanow et al. (5,367,494) .

19. As to claim 7, limitation of claim 6 have been discussed in program ph above, therefore it will not be repeated herein. Tanaka showed a write enabling signal for each memory caches (memory banks). Tanaka did not specifically show that his write signal was used for enabling and disabling of the subset of memory banks as claimed. However, Shebanow taught a system for enabling a subset of memory banks (see Abstract , see also the enabling of memory banks on the control value A and B in col.11, lines 5-68, col.12, lines 1-27). It would have been obvious to one of

ordinary skill in the art to sue Shebanow in Tanaka for enabling/disabling the subset of memory banks as claimed because the use of Shebanow could provide Tanaka the ability to accept and send data from a plurality of memory sets at a given cycle, therefore, increasing the bandwidth of the storage access control , and because Tanaka also taught to provide a plurality of processing units with corresponding memory caches (the banks) for execution in parallel (see col.3, lines 52-63), which was a suggestion of the need for activating a subset of memory banks (see the memory caches) in order to provide data to the plurality of processing units in parallel, and for doing so, provide a motivation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H PAN
PRIMARY EXAMINER
GROUP